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09/385,959	08/30/1999	TOSHIHARU YANAGIDA	P99.1318	9858
26263 7590 10/25/2007 SONNENSCHN NATH & ROSENTHAL LLP P.O. BOX 061080 WACKER DRIVE STATION, SEARS TOWER CHICAGO, IL 60606-1080			EXAMINER GRAYBILL, DAVID E	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Application Number: 09/385,959
Filing Date: August 30, 1999
Appellant(s): YANAGIDA, TOSHIHARU

MAILED
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GROUP 2800

Christopher P. Rauch
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4-10-6 appealing from the Office action mailed 8-4-5.

(1) Real Party in Interest

Art Unit: 2822

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

Appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows: The claims do not stand "as allegedly" being unpatentable. Rather, they stand as being unpatentable.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Art Unit: 2822

2002/0106832	HOTCHKISS et al.	8-2002
6,227,436	NISHIKAWA et al.	5-2001
6,187,682	DENNING et al.	2-2001
6,114,187	HAYES	9-2000
5,147,084	BEHUN et al.	9-1992
5,068,040	JACKSON	11-1991
4,807,021	OKUMURA	2-1989

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

In the rejections infra, generally, reference labels are recited only for the first recitation of identical elements.

Claims 7, 8, 10, 11, 16 and 19-21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hayes (6114187), Hotchkiss (2002/0106832) and Behun (5147084).

At column 5, line 23 to column 7, line 48; column 9, lines 1-35; column 10, lines 18-29; and claim 3, Hayes discloses a method of producing a semiconductor apparatus, the method comprising the steps of: forming metal ball bumps 3, (column 10, lines 25-27: "ball of solder") in direct contact with a circuit pattern 2 of a semiconductor device 1 formed on a semiconductor substrate 17 in a wafer state; forming a resin film 4 on a circuit pattern forming surface of said semiconductor device so as to seal spaces between

Art Unit: 2822

said metal ball bumps and to become thinner than a height of the metal ball bumps ("ablated surface 23 seen in FIG. 2d is created slightly below the top 7 of each column 3," and claim 3); cleaning the surfaces of the metal ball bumps projecting out from the resin film; after the cleaning step, forming eutectic solder layers 9 different in composition from the metal ball bumps on the surfaces of the metal ball bumps; after the forming solder layers step, cutting the semiconductor wafer into unit semiconductor chips 1, each semiconductor chip having at least one of said semiconductor device; and after the cutting step, mounting at least one of the semiconductor chips on a mounting "substrate" (not labeled) from a bump forming surface side of the semiconductor chip so as to connect the eutectic solder layers of the semiconductor chip to the mounting substrate "flip-chip fabrication."

Although Hayes discloses mounting at least one of the semiconductor chips on a mounting substrate, Hayes does not appear to explicitly disclose a mounting board substrate.

Nonetheless, as cited supra, Hotchkiss discloses mounting a semiconductor chip 112 on a mounting "board" (not labeled) substrate. In addition, it would have been obvious to combine the process of Hotchkiss with the process of Hayes because it would provide the mounting substrate of Hayes.

Art Unit: 2822

Because appellant continues to insist on the unique interpretation that Hayes does not disclose that the bumps 3 are ball bumps, and because Hayes is already applied in combination with Hotchkiss for disclosure of a mounting board substrate, in the alternative, Hayes is applied further in combination with Hotchkiss for a disclosure of metal ball bumps 3. In particular, Hayes discloses forming metal column bumps 3 in direct contact with the circuit pattern 2 for use with a flip-chip semiconductor. Furthermore, at paragraphs 33-36, and claims 13 and 14, Hotchkiss discloses that metal column bumps and metal ball bumps are alternative and equivalent solder bumps for use with a flip-chip semiconductor. Therefore, as reasoned from well established legal precedent, it would have been obvious to substitute the metal ball bumps of Hotchkiss for the metal columns of Hayes. See *In re May* (CCPA) 136 USPQ 208 (It is our opinion that the substitution of Wille's type seal for the cement of Hallauer in Figure 1 would be obvious to persons of ordinary skill in the art from the disclosures of these references, merely involving an obvious selection between known alternatives in the art and the application of routine technical skills.); *In re Cornish* (CCPA) 125 USPQ 413; *In re Soucy* (CCPA) 153 USPQ 816; *Sabel et al. v. The Wickes Corporation et al.* (DC SC) 175 USPQ 3; *Ex parte Seiko Koko Kabushiki Kaisha Co.* (BdPatApp&Int) 225 USPQ 1260; and *Ex parte Rachlin* (BdPatApp&Int) 151 USPQ 56. See also *Smith v. Hayashi*, 209

Art Unit: 2822

USPQ 754 (Bd. of Pat. Inter. 1980) (However, there was evidence that both phthalocyanine and selenium were known photoconductors in the art of electrophotography. "This, in our view, presents strong evidence of obviousness in substituting one for the other in an electrophotographic environment as a photoconductor." 209 USPQ at 759.). An express suggestion to substitute one equivalent component or process for another is not necessary to render such substitution obvious. In re Fout, 675 F.2d 297, 213 USPQ 532 (CCPA 1982). "It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose.... [T]he idea of combining them flows logically from their having been individually taught in the prior art." In re Kerkhoven, 626 F.2d 846, 850, 205 USPQ 1069, 1072 (CCPA 1980) (citations omitted). See also In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960); Ex parte Quadranti, 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992).

Hayes also does not appear to explicitly disclose mounting the semiconductor chip on the mounting board with the resin film directly contacting the semiconductor chip and not directly contacting the mounting board.

Notwithstanding, at column 3, lines 38-62, column 5, lines 7-12, and column 5, line 41 to column 6, line 15, Behun discloses mounting a semiconductor chip 10 on a mounting board 11 with the

Art Unit: 2822

resin film 20 directly contacting the semiconductor chip and not directly contacting the mounting board. Furthermore, it would have been obvious to combine the processes of Behun with the applied prior art because, as taught by Behun, it would facilitate reworkability and heat dissipation.

As cited, Hayes also discloses a process of production of a semiconductor apparatus wherein, in said cleaning step, the surfaces are cleaned by removing components inviting a rise in a connection resistance and a decline in a joint strength at least at a connection interface; in said cleaning step, any resin film components deposited on said bumps are removed; in said cleaning step, oxides on said bump surfaces are removed; in said cleaning step, the cleaning of the surfaces of the bumps is performed by irradiating a laser beam; the metal ball bumps formed in the first step are solder bumps; said solder bumps have a melting point higher than a melting point of said eutectic solder and said eutectic solder layers are comprised of a eutectic solder; and in said forming solder layers step, the eutectic solder layers are formed by a printing method, plating method, or transfer method.

To further clarify the disclosures wherein the surfaces are cleaned by removing components inviting a rise in a connection resistance and a decline in a joint strength at least at a connection interface, and oxides on said bump surfaces are removed, it is noted that these processes are inherent results of the

Art Unit: 2822

cleaning process of Hayes wherein, "The laser ablation process will also clean off top 7 of each column 3 to expose uncontaminated solder."

Claims 12, 13 and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hayes, Hotchkiss and Behun as applied to claim 7, and further in combination with Nishikawa (6227436) and Denning (6187682).

The combination of Hayes, Hotchkiss and Behun does not appear to explicitly disclose a process of production of a semiconductor apparatus wherein, in said cleaning step, the cleaning of the surfaces of the bumps is performed by plasma cleaning; said plasma cleaning is at least sputter etching by discharge plasma of an inert gas; and the cleaning of the surfaces of the bumps is performed under a reduced pressure atmosphere, an inert gas atmosphere, or a reducing gas atmosphere.

Nevertheless, at column 5, line 62 to column 6, line 67, Nishikawa discloses a process of production of a semiconductor apparatus 1 wherein cleaning of the surfaces of bumps 9 is performed by sputter etching of an inert gas ("argon"). Moreover, it would have been obvious to combine the process of Nishikawa with the process of the applied prior art because it would enable cleaning of the surfaces of the bumps 3.

However, the combination of Hayes, Hotchkiss, Behun and Nishikawa does not appear to explicitly disclose that the sputter etching is by discharge plasma.

Regardless, at column 2, line 66 to column 5, line 50, Denning discloses a process of sputter etching by discharge plasma. Furthermore, it would have been obvious to combine the process of Denning with the process of the applied prior art because it would enable the sputter etching.

Claims 14 and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hayes, Hotchkiss, Nishikawa, Behun and Denning as applied to claim 12, and further in combination with Okumura (4807021).

The prior art applied to claim 12 does not appear to explicitly disclose a process of production of a semiconductor wherein said plasma cleaning is at least oxygen plasma treatment and then sputter etching by discharge plasma of an inert gas; and wherein said plasma cleaning is at least oxygen plasma treatment and then sputter etching by discharge plasma of a reducing gas.

However, as cited supra, Denning discloses a process wherein plasma cleaning is sputter etching by discharge plasma of an inert and a reducing gas. Moreover, it would have been obvious to combine the process of Denning with the process of the applied prior art because it would enable cleaning. Also, at column 5, lines 32-44, Okumura discloses a process of production of a

Art Unit: 2822

semiconductor apparatus wherein plasma cleaning is at least oxygen plasma treatment. In addition, it would have been obvious to combine the process of Okumura with the process of the applied prior art because it would enable cleaning.

Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Hayes, Hotchkiss and Behun as applied to claim 7, and further in combination with Jackson (5068040).

The combination of Hayes, Hotchkiss and Behun does not appear to explicitly disclose wherein, in said cleaning step, the cleaning of the surfaces of the bumps is performed while applying a gas jet to the bumps to peel off the unnecessary components which are then sucked away.

Notwithstanding, at column 4, line 44 to column 5, line 33; and column 7, line 46 to column 8, lines 49, Jackson discloses a process wherein the cleaning of the surfaces of a semiconductor apparatus is performed while applying a gas jet to the apparatus to peel off the unnecessary components which are then sucked away. Additionally, it would have been obvious to combine the process of Jackson with the process of the applied prior art because it would enable cleaning.

(10) Response to Argument

Appellant asserts, "Hayes fails to teach forming metal ball bumps in direct contact with a circuit pattern."

Art Unit: 2822

This assertion is respectfully traversed because, as elucidated in the rejection, at column 10, lines 18-29, Hayes explicitly discloses that metal columns 3 can take the shape of metal ball bumps: "Generally, things that reduce the freezing rate tend to create a column that is wider and not as tall. If a longer time is provided between drops (normal operation is around 200 drops per second) the preceding drops have more time to freeze before the next drop arrives. This tends to build a narrower taller column. If the drop temperature is higher or there is less time between drops, the column tends to be fatter and lower. If the drops are very close together in time, they will solidify into one big ball of solder [emphasis added]." And, at column 9, lines 11-13, Hayes discloses that the metal columns (which can take the shape of metal ball bumps) are in direct contact with a circuit pattern 2; "Row C shows the addition of a plurality of solder columns 3, each on a pad 2, to represent the step of FIG. 1b."

Appellant further argues, "Hotchkiss fails to teach eutectic solder layers formed on its metal ball bumps 114," and, "Behun also fails to disclose forming metal ball bumps in direct contact with a circuit pattern and also fails to disclose forming eutectic solder layers on its metal ball bumps." Thereby concluding, "Therefore, none of the cited references, taken individually, teaches eutectic solder layers formed on metal bumps."

Art Unit: 2822

This argument is respectfully deemed unpersuasive because Hotchkiss and Behun are not individually applied to the rejections for these disclosures. Instead, as elucidated supra, Hayes is applied both individually and in combination to the rejections for these disclosures.

In addition, appellant alleges, "The Examiner argues that both Hayes's solder columns and Hotchkiss' [sic] metal ball bumps provide a conductive path and, therefore, one skilled in the art would have been motivated by Hayes in view of Hotchkiss to interchange Hayes's solder columns with Hotchkiss' metal ball bumps."

This allegation is respectfully traversed because there is no such argument of record. Rather, it is argued, "Hayes discloses forming metal column bumps 3 in direct contact with the circuit pattern 2 for use with a flip-chip semiconductor. Furthermore, at paragraphs 33-36; and claims 13 and 14, Hotchkiss discloses that metal column bumps and metal ball bumps are alternative and equivalent solder bumps for use with a flip-chip semiconductor. Therefore, as reasoned from well established legal precedent, it would have been obvious to substitute the metal ball bumps of Hotchkiss for the metal columns of Hayes."

Relatedly, appellant contends, "Hayes clearly states that it uses solder columns instead of solder ball bumps to avoid accidentally short-circuiting its underlying electrical pads

Art Unit: 2822

(Hayes, col. 9, line 62 - col. 10, line 9). Therefore, Hayes specifically teaches away from forming metal ball bumps on its electrical pads, and teaches instead to use solder columns."

This contention is respectfully traversed because there is no such disclosure at the cited disclosure, nor elsewhere in the disclosure. Instead, the cited disclosure discloses the use of solder column 64, 3' **in addition to** (not "instead of") solder ball bumps 9 **and** solder column 3 so that there is no interference between solder ball bumps 9 on the columns. Therefore, there is no "teaching away from forming metal bumps on its electrical pads" in Hayes. Also, as elucidated supra, Hayes explicitly discloses that columns 3, can take the form of a "ball of solder." In any case, the contention that Hayes teaches away from the claimed invention is respectfully traversed because, at the cited disclosure, Hayes merely discloses one embodiment of numerous embodiments, and disclosed embodiments do not necessarily constitute a teaching away from a broader disclosure or other embodiments. In re Susi, 169 USPQ 423 (CCPA 1971). "A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." In re Gurley, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994). A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including nonpreferred embodiments. Merck & Co. v. Biocraft Laboratories, 874 F.2d 804, 10 USPQ2d 1843 (Fed.

Art Unit: 2822

Cir.), cert. denied, 493 U.S. 975 (1989). To further clarify, a prior art opinion that a claimed invention is not preferred for a particular limited purpose, does not preclude utility of the invention for that or another purpose, or even preferability of the invention for another purpose. Moreover, even a teaching away from a claimed invention does not necessarily render the invention patentable. See *Celeritas Technologies Ltd. v. Rockwell International Corp.*, 150 F.3d 1354, 1361, 47 USPQ2d 1516, 1522-23 (Fed. Cir. 1998), where the court held that the prior art anticipated the claims even though it taught away from the claimed invention. "The fact that a modem with a single carrier data signal is shown to be less than optimal does not vitiate the fact that it is disclosed." Similarly, in *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997) applicant argued that the prior art taught away from use of a protective layer for a reflective article having a thickness within the claimed range of "50 to 100 Angstroms." Specifically, a patent to Zehender, which was relied upon to reject applicant's claim, included a statement that the thickness of the protective layer "should be not less than about [100 Angstroms]." The court held that the patent did not teach away from the claimed invention. "Zehender suggests that there are benefits to be derived from keeping the protective layer as thin as possible, consistent with achieving adequate protection. A thinner coating reduces light absorption

Art Unit: 2822

and minimizes manufacturing time and expense. Thus, while Zehender expresses a preference for a thicker protective layer of 200-300 Angstroms, at the same time it provides the motivation for one of ordinary skill in the art to focus on thickness levels at the bottom of Zehender's suitable range - about 100 Angstroms - and to explore thickness levels below that range. The statement in Zehender that [i]n general, the thickness of the protective layer should be not less than about [100 Angstroms] falls far short of the kind of teaching that would discourage one of skill in the art from fabricating a protective layer of 100 Angstroms or less. [W]e are therefore not convinced that there was a sufficient teaching away in the art to overcome [the] strong case of obviousness made out by Zehender." See MPEP 2144.05II and MPEP 2145, paragraph X.D..

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

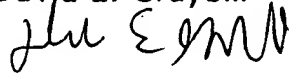
For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Application/Control Number: 09/385,959
Art Unit: 2822

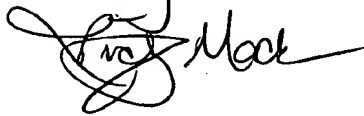
Page 16

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